PATENT
Customer No. 22,852
Attorney Docket No. 04329.1952-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Yoshitaka Tsunashima et al.	)	Group Art Unit: 2814
	)	
Application No.: 09/688,989	)	Examiner: Rao, Shrinivas H.
	)	
Filed: October 17, 2000	)	
	)	
For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE TO NOTICE OF NON-COMPLIANT AMENDMENT

In response to the Notice of Non-Compliant Amendment dated February 26, 2004, the period for response to which extends through March 26, 2004, Applicants submit a revised "**AMENDMENTS TO THE CLAIMS**" section of the Amendment filed on November 18, 2003. The revised "**AMENDMENTS TO THE CLAIMS**" section includes a complete listing of all claims, including canceled claims 1-26 which were inadvertently omitted from the listing of the claims submitted with the Amendment filed on November 18, 2003. Claims 1-11 and 13-25 were canceled via the Transmittal Letter accompanying the filing of this application, and claims 12 and 26 were canceled in the Amendment filed July 12, 2001 for this application.

Please associate this corrected "**AMENDMENTS TO THE CLAIMS**" section with the application, grant any extensions of time required to enter this response, and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: March 17, 2004

By: Richard V. Burgujian Reg 24,014
for Richard V. Burgujian
Reg. No. 31,744

AMENDMENTS TO THE CLAIMS:

Please amend claims 27, 28, and 31-33, as indicated below.

This listing of claims will replace all prior versions and listings of claims in the application:

1. - 26. (Canceled)

27. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate including a first and second region separated by an isolation element;

a first transistor formed on [[a]] the first region of the substrate and including a first insulation film and a first gate electrode arranged along a first direction; and

a second transistor formed on [[a]] the second region of the substrate and including a second insulation film and a second gate electrode arranged along the first direction,

wherein a side wall of the [[said]] first gate electrode ~~at one end of a channel direction~~ is connected to a side wall of the [[said]] second gate electrode ~~at one end of the channel direction~~ above the isolation element when viewed from a direction perpendicular to the first direction.

28. (Currently Amended) A device according to claim [[27]] 33, wherein ~~a part of the side wall of the first gate electrode is only connected to a part of the side wall of the second gate electrode and said part of the side wall of the first gate electrode and said part of the side wall of the second gate electrode are~~ the side insulator film is substantially perpendicular to a surface of said semiconductor substrate.

29. (Canceled)

30. (Previously Presented) A device according to claim 28, wherein at least one of said first and second gate electrodes is formed by a damascene gate process.

31. (Currently Amended) A device according to claim [[27]] 33, wherein ~~said first transistor includes a first insulator film, said second transistor includes a second insulator film,~~ said first ~~insulator~~ insulation film is thinner than said second ~~insulator~~ insulation film, said first transistor ~~is included in~~ forms a logic circuit, and said second transistor ~~is included in~~ forms a memory cell.

32. (Currently Amended) A device according to claim [[27]] 33, wherein top surfaces of said first and second gate electrodes ~~and a connection layer~~ are coplanar.

33. (Currently Amended) A device according to claim 27, wherein said second transistor further comprises ~~a gate insulator film formed on the substrate,~~ a polysilicon layer formed on the second insulation film formed on the substrate ~~gate insulator film~~, and a side insulator film formed on a side wall of the ~~gate insulator~~ second insulation film and a side wall of the polysilicon layer, said second gate electrode is formed on the polysilicon layer, ~~and said~~ the side wall of said first gate electrode is directly connected to [[the]] a side wall of said second gate electrode and ~~a side wall of said side insulator film~~ connected to the side wall of the second insulation film and the side wall of the polysilicon layer via the side insulator film.

C.F.R. §1.28(b)

Once status as a small entity has been established in an application or patent, s as a small entity may thereafter be paid in that application or patent without ard to a change in status until the issue fee is due or any maintenance fee is due. ification of any change in status resulting in loss of entitlement to small entity tus must be filed in the application or patent prior to paying, or at the time of ing, the earliest of the issue fee or any maintenance fee due after the date on ch status as a small entity is no longer appropriate pursuant to §1.9 of this part. notification of change in status may be signed by the applicant, any person horized to sign on behalf of the assignee, or an attorney or agent of record or ing in a representative capacity pursuant to §1.34(a) of this part.

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. 37 C.F.R. §1.28(b)*.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

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